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SEU Sensitivity of Junctionless Single-Gate SOI MOSFETs-based 6T SRAM Cells Investigated by 3D TCAD Simulation

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Abstract

The Junctionless (JL) Single-Gate SOI (JL-SOI) technology is potentially interesting for future ultra-scaled devices, due to a simplified technological process and reduced leakage currents. In this work, we investigate the radiation sensitivity of JL-SOI MOSFETs and 6T SRAM cells. A detailed comparison with JL Double-Gate (JL-DG), inversion-mode (IM) SOI (IM-SOI), and IM-DG MOSFETs has been performed. 3-D simulations indicate that JL-SOI MOSFETs and SRAM cells are naturally less immune to radiation than the other structures.

Keywords
Junctionless Single-Gate SOI MOSFET, SEU, SEE, bipolar amplification, threshold LET SRAM cell, Double-Gate MOSFET, SOI

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1. Introduction

As the MOSFET is scaling down, the sensitivity of integrated circuits to radiation coming from space or present in the terrestrial environment has been found to seriously increase [1]. For ultra-scaled devices entering in the area of nanoelectronics, natural radiation at ground level is presently inducing one of the highest failure rates of all reliability concerns [2]. In particular, ultra-scaled memory integrated circuits have been found to be more sensitive to single-event-upset (SEU) induced by ionizing particles.

To meet the roadmap requirements in the nanometre scale, several promising technological solutions have been proposed, such as the Fully-depleted Single-Gate SOI technologies (FDSOI) fabricated with ultra-thin silicon bodies [3]. FDSOI devices show enhanced performances in terms of channel potential control, reducing short-channel (SCE) and floating body effects (FBE). A new concept of MOSFET without junctions, called junctionless (JL) MOSFET has been proposed these last years and experimentally validated [4-7]. A JL MOSFET designed with a single-gate SOI structure (JL-SOI, Fig. 1a) is an SOI transistor with the same type of semiconductor throughout the entire silicon film, including the source, channel and drain regions. JL-SOI devices present a real advantage since their fabrication process is simplified compared to the conventional process: there are no doping gradients in the device [6] and no semiconductor-type inversion. In addition, the junction leakage currents are totally suppressed and the off-state current (I_{OFF}) is uniquely controlled by the gate, which could be very attractive for ultra-short devices.

The JL-SOI technology is then potentially interesting for future ultra-scaled devices, due to the simplified technological process without junction engineering and reduced leakage current. JL-SOI MOSFETs have been already fabricated, but experimental studies concerning their sensitivity to radiation are not yet available in literature. In the context of microelectronics characterized by industrial needs for high-reliable circuits in a wide area of applications, it is important to investigate in detail the sensitivity to radiation of the JL-SOI technology with respect to the radiation sensitivity of other more conventional technologies envisaged for high-reliability concerns, such as the inversion-mode (IM) FDSOI (IM-SOI, Fig. 1b) and inversion-mode double-gate (IM-DG) MOSFETs [8-9]. These last devices are very interesting for the nanometer scale, since they present a very good control of parasitic short channel effects (SCE) [10], no parasitic doping fluctuation effects due to the intrinsic nature of the film, increased carrier mobility and drain current [11] and high probability of

ballistic transport in the channel [12-14].

From a radiation-sensitivity point of view, the high doping level in the film of a JL MOSFET could have a negative impact on its immunity to single events, because floating body effects are expected to be strong. This was confirmed by our previous works [15-16] concerning the radiation-induced transient behavior of JL Double-Gate (JL-DG) MOSFETs. In spite of its double-gate configuration, JL-DGFET should be more sensitive to radiation than IM-DGFET for which the channel is intrinsic. The transient response of IM-DG devices under heavy-ion irradiation has been studied by 3-D numerical simulation in [17-20]. These previous studies demonstrated that IM-DG shows a better resistance to radiation than IM-SOI, due to the enhanced control of the film potential by the two connected gates which reduces floating-body effects. The bipolar amplification of JL-DG was studied in [15] and compared to that of IM-DG with similar geometrical parameters. In that previous work, we have shown that JL-DG is characterized by a higher bipolar gain than IM-DG, due to stronger floating-body effects. In addition, results obtained in [16] have shown that JL-DG SRAM cell is characterized by a lower critical charge than IM-DG cell, but higher than IM-SOI SRAM.

In the present work, we investigate, for the first time, the radiation sensitivity of JL-SOI, in terms of bipolar gain of individual devices and SEU sensitivity of six-transistor (6T) SRAM cells. A detailed comparison with JL-DG, IM-SOI and IM-DG devices and 6T SRAM cells has been also performed.

2. Simulation details

Figure 1 shows the schematic 3-D descriptions of the simulated JL-SOI and IM-SOI devices. JL-SOI devices are designed with 100 nm gate width, 6 nm-thick silicon film and 0.9 nm-thick gate oxide. The entire silicon film is uniformly n-type doped at 1×10^{19} cm^{-3}; there are no highly-doped source/drain regions. A 10 nm-thick buried oxide (BOX) and a thick silicon substrate doped at 5×10^{18} cm^{-3} have been also considered. The very thin buried oxide is necessary to minimize the short channel effects in this JL-SOI device. It should be noted that the channel thickness has to be sufficiently small in order to make possible the complete depletion of the silicon film and to be able to cut-off the device [4]. This condition is satisfied for the doping level and the film thickness considered here. IM-SOI devices (Fig. 1b) have an intrinsic channel; source and drain regions are highly n-type doped and the doping profile in these regions is uniform. The silicon film, BOX and silicon substrate of IM-SOI have the

same geometrical parameters as those of JL-SOI. The silicon substrate is lowly-doped at 10^{16} cm^{-3}. IM-DG and JL-DG structures are based on real devices reported in [21]. The silicon film of IM-DG and JL-DG has the same geometrical parameters and doping profiles as the silicon film of IM-SOI and JL-SOI, respectively, with the notable exception that two gates connected together control the channel potential. These four different structures have been first simulated with 20 nm-channel length, considering a power supply voltage of 0.75 V. These devices have been calibrated on the ITRS LP [22]; to facilitate the comparison, the gates work functions have been finely tuned to achieve the same I_{OFF} for all devices. Secondly, additional simulations have been carried out for other channel lengths and power supply voltages.

3-D numerical simulations have been performed with the DESSIS device simulator from Synopsis Inc. [23]. The main models used in simulation are: SRH and Auger recombination models, Fermi-Dirac carrier statistics, hydrodynamic model for the carrier transport, mobility model including the dependence on the carrier energy, lattice temperature and doping level and impact ionization model depending on carrier energy. Realistic values have been used for the main electrical parameters of the models used in simulation, such as electrons and holes lifetimes and low field carrier mobility. The ion strike was simulated using the DESSIS HeavyIon module [23]. The electron-hole pair column created in the device by the ion strike is modeled using a carrier-generation function which has a Gaussian radial distribution with a characteristic radius of 20 nm and a Gaussian time distribution, centered on 10 ps and having a characteristic width of 2 ps.

3. Static characteristics of individual devices

The simulated steady-state drain current characteristics of JL-SOI, IM-SOI, JL-DG and IM-DG are plotted in Fig. 2. The devices have the same off-state current, but different subthreshold swings and on-state currents. While double-gate devices (both JL-DG and IM-DG) have near ideal subthreshold swings (65 mV/dec), SOI devices have a much higher subthreshold swing (90 mV/dec) because the single-gate configuration reduces the control by the gate of the channel potential and increases the parasitic short-channel effects compared to a double-gate configuration. JL-SOI has the lowest on-state current because the highly-doped silicon film degrades the mobility. The highest on-state current is obtained in IM-DG, due to the combination of a double-gate structure and an intrinsic channel; this structure has the advantage to maximize the carrier mobility and the gate-channel coupling.

4. Single-event transients

4.1. Drain current, collected charge and bipolar gain

Figure 3 shows the drain current transient resulting from an ion hit in the channel center of JL-SOI and IM-SOI devices. Time variations of the collected charge are also reported on the same figure. The drain current transient peak and width are higher in JL-SOI than in IM-SOI, probably due to a higher bipolar gain. In addition, the drain current decay after the ion strike is slower for JL-SOI than for IM-SOI. The reason is that the floating body effects are more important in JL-SOI than in IM-SOI, due to the high doping level in the JL-SOI film (since the device channel is intrinsic in IM-SOI). The collected charge and the bipolar amplification as function of the ion LET are plotted in Figs. 4a and 4b, respectively. The values obtained in [15] for JL-DG and IM-DG devices are also reported in these figures for comparison. As expected, the collected charge and the bipolar gain are higher in JL-SOI than in IM-SOI due to stronger FBE. Compared to the JL-DG structure having the same film doping level, JL-SOI device presents a higher bipolar gain for all LET values. This is due to a less effective film potential control in this structure with a single-gate compared to the double-gate control of the JL-DG device. The bipolar gain decreases when the LET increases because the parasitic bipolar transistor enters in the high-injection regime. At very high LET value, the bipolar gain in JL-SOI decreases rapidly and becomes close to the values obtained in IM-SOI, JL-DG and IM-DG.

4.2. Dependence on the ion hit location

We also studied the dependence of the bipolar gain on the ion hit location along the channel (x axis). Several locations are considered between the source contact (x=0) and the drain contact (x=60 nm), as illustrated in Fig. 5a. The 3-D profile of the heavy ion charge density in the silicon film is also shown in Fig. 5a for an ion hitting the film at x=30 nm (channel center). The current transient have been simulated for each x location and the collected charge was extracted from this transient. The bipolar gain is then obtained at a given LET for each x value. Figure 5b plots the bipolar gain dependence on the ion hit location for the four studied devices. The bipolar gain is always higher in JL-SOI than in IM-SOI, but has similar dependences on the ion hit location for all devices.

5. SEU in 6T SRAM cells: critical charge and threshold LET

For the four technologies, the 6 transistors of the SRAM cell (Fig. 6) were entirely simulated in the 3-D device domain with the Synopsis/DESSIS module and were connected via the Mixed-Mode module [23]. Only the OFF-state NMOS transistor was struck by an ionizing particle (see Fig. 6), this particular case corresponding to the most effective scenario to disturb the cell and to flip its logical state.

Before simulating the SRAM cell, we have determined for each technology the worst-case condition in terms of x location (along the channel) of the ion hit in the OFF-state NMOS. The worst-case location is the x location for which the collected charge is the highest. Then, the SEU LET threshold obtained in this point will be the smallest LET for which the SRAM cell flips. To find the worst-case location, the current transient is simulated for each x location and the collected charge is extracted from this transient. The bipolar gain is then obtained at a given LET for each x value (according to a similar analysis to that presented in section 4.2). The worst-case x locations were found to be x=35 nm for JL-SOI and x=40 nm for IM-SOI devices. In the following, we used these worst-case locations for the SRAM cell simulations.

5.1. Simulation of SRAM cells

In a first time, we simulated the behavior of the SRAM cell built with JL-SOI transistors when an ionizing particle strikes the OFF-state NMOS transistor. Figure 7a shows the time variation of voltages extracted at nodes “A” and “B” (V_A and V_B). The corresponding time variations of the current and the collected charge measured at the drain (node “A”) of the impacted transistor for three values of the ion LET are shown in Fig. 7b. When the ion LET increases the current peak increases because the capacitive effect induced by the ion is stronger [16]. The charge collected at node “A” also increases (it proportionally depends on the ion LET). The current transient induced by the ionizing particle disturbs the voltages of nodes “A” and “B” and the disturbance is stronger when the ion LET increases. Figure 7a shows that, for LET=0.5 and 0.8 MeV·cm^2/mg, V_A and V_B are disturbed, but their values do not change at the end of the transient. For these LET values the state of the SRAM cell is not modified (the cell does not flip). On the contrary, for LET=1.5 MeV·cm^2/mg, the values of V_A and V_B change with respect to their initial value and the SRAM cell flips. In this case, the ion LET is sufficiently high to induce a collected charge larger than the critical charge of the

cell and to cause the SRAM cell upset.

Secondly, we investigate the behavior of SRAM cells made up of JL-SOI and IM-SOI. Time variations of the voltages V_A and V_B for LET=3 MeV·cm^2/mg are shown in Fig. 8 for JL-SOI and IM-SOI SRAM cells. For this LET value, the JL-SOI SRAM cell has flipped, while the IM-SOI SRAM cell did not flip. This result gives a first indication on the radiation hardness of JL-SOI technology: the SEU threshold LET of JL-SOI SRAM cell will be lower than that of IM-SOI, which means that the JL-SOI is more sensitive to radiation than the IM-SOI technology.

5.2. Threshold LET and critical charge

To refine the analysis, we obtained the SEU threshold LET (LET_{th}) of each cell by varying the ion strike LET until the SRAM cell was observed to upset. As expected, the critical charge (Q_{crit}=0.126 fC) and the threshold LET (LET_{th}=1.32 MeV·cm^2/mg) are lower for the JL-SOI SRAM than for IM-SOI SRAM cell (Q_{crit}=0.205 fC and LET_{th}=3.15 MeV·cm^2/mg, [16]). In order to explain these results, we remind that Q_{crit} increases with the equivalent capacitance of the struck node (C_N), with the supply voltage (V_{DD}) and with the maximum current of the on-state PMOS transistor (I_{PMOS}), as explained in [24]. In our study, all cells are operating at the same V_{DD}. C_N is the same for JL-SOI and IM-SOI SRAM cells, but I_{PMOS} is lower in JL-SOI than in IM-SOI; this then explains why Q_{crit} is lower in JL-SOI than in IM-SOI SRAM cell. Q_{crit} and LET_{th} of JL-SOI are also lower than those corresponding to JL-DG (Q_{crit}=0.309 fC and LET_{th}=3.64 MeV·cm^2/mg) and IM-DG (Q_{crit}=0.51 fC and LET_{th}=7.48 MeV.cm^2/mg) obtained in [16].

5.3. Dependence on the channel length, power supply and film doping level

To study more in depth the radiation hardness of these SRAM cells, we investigated the dependence of the SEU threshold LET on the channel length, power supply and film doping level (for JL-SOI SRAM cells). Figure 9 presents the threshold LET values obtained for two channel lengths (L=20 nm and L=50 nm) and for all devices considered in this work. 50 nm-gate length devices have the same geometrical and doping parameters as those of 20-nm gate length devices, excepted for the channel lengths. Our simulations showed that the critical charge and the threshold LET (Fig. 9) are reduced when the channel length decreases for all technologies, in accordance with previous results [25].

SRAM simulations have been performed on 20-nm length JL-SOI structures for different power supply values (all geometrical and doping parameters are the same as in section 2, only the power supply varies). As expected from theoretical predictions (explained before), the critical charge increases with the power supply. Our simulations give Q_{crit}=0.175 fC for V_{DD}=0.9 V and Q_{crit}=0.21 fC for V_{DD}=1.1 V. The threshold LET also increases: we obtained LET_{th}=1.8 MeV·cm^2/mg for V_{DD}=0.9 V and LET_{th}=2.04 MeV·cm^2/mg for V_{DD}=1.1 V.

SRAM simulations have been also conducted on 20-nm gate length JL-SOI technology with different film doping levels. Three additional doping levels have been considered: 5×10^{18}, 1.5×10^{19} cm^{-3} and 2×10^{19} cm^{-3}. The gate workfunctions of these devices have been tuned in order to obtain the same I_{off} current as the 20-nm gate length JL-SOI structure having the silicon film doped at 1.5×10^{19} cm^{-3} (other geometrical and doping parameters are the same as those considered in section 2). Critical charges and threshold LETs, presented in Table I, decrease when the doping level increase from 5×10^{18} to 2×10^{19} cm^{-3}. To explain these results, the behavior of individual devices has been analyzed. Our simulations showed that when the film doping of JL-SOI increases, the floating body effects are enhanced, the drain current transient is longer and the impact ionization increase. These results are in perfect agreement with those obtained in [15] for JL-DG MOSFETs. Then, both the collected charge and the bipolar amplification increase, which leads to a lower critical charge needed to flip the SRAM cell and to a lower threshold LET.

6. Conclusion

In this paper we have presented the transient response to heavy ion irradiation of JL-SOI devices and SRAM cells. Our results show that the bipolar amplification is higher in JL-SOI devices than in conventional IM-SOI because the floating body effects and the impact ionization are enhanced due to the highly doped channel. In addition, JL-SOI SRAM cell is characterized by a lower critical charge and threshold LET than IM-SOI cell. Compared to the JL-DG structure having the same film doping level, JL-SOI device presents a higher bipolar gain, lower critical charge and lower threshold LET. This is due to a less effective film potential control in JL-SOI with a single gate compared to the double-gate control of the JL-DG device. In addition, when the film doping of individual devices increases the radiation hardness of the JL-SOI SRAM cell is degraded. From these results, we could expect a worse immunity to single-event phenomena of JL-SOI devices and circuits compared to that of IM-

SOI and JL-DG MOSFETs.

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Figure and Table Captions

Fig. 1. Schematic description of the simulated JL-SOI (a) and IM-SOI (b) MOSFETs. For a better view spacers and isolation oxides are not shown. The doping level distribution in each device is shown and the main geometrical parameters are defined. The position of the ion strike is indicated by the arrow; the ion strikes vertically in the middle of the channel and in a direction parallel to the z axis.

Fig. 2. Drain current as a function of gate voltage for JL-SOI, IM-SOI, JL-DG and IM-DG. The gate workfunction of each device has been tuned to obtain the same I_{OFF}.

Fig. 3. Drain current transient and collected charge in JL-SOI and IM-SOI for an ion hit in the channel center.

Fig. 4. Collected charge and bipolar amplification as function of LET in JL-SOI and IM-SOI MOSFETs for an ion hit in the channel center.

Fig. 5. (a) 3-D profile of heavy-ion charge density in the silicon film of JL-SOI for an ion hit at x=30 nm and LET=1 $MeV \cdot cm^2/mg$. Other positions for the ion strike considered in this work are also indicated. For a better view of the film, gate material, spacers and isolation oxide are not shown. (b) Bipolar gain in JL-SOI, IM-SOI, JL-DG and IM-DG as a function of the ion hit location.

Fig. 6. Schematics of the SRAM cell simulated in this work. The particle hits the OFF-state

NMOS transistor (NMOS 2).

Fig. 7. JL-SOI SRAM cells: (a) time variation of voltages V_A and V_B and (b) current transient and collected charge at node "A".

Fig. 8. Time variation of V_A and V_B in JL-SOI and IM-SOI SRAM cells at LET=3 MeV·cm^2/mg.

Fig. 9. Threshold LET of JL-SOI, IM-SOI, JL-DG and IM-DG SRAM cells for two channel lengths, L=20 and 50 nm.

Table I. Critical charge and threshold LET in 20-nm gate length JL-SOI SRAM cells for different film doping levels of individual devices.

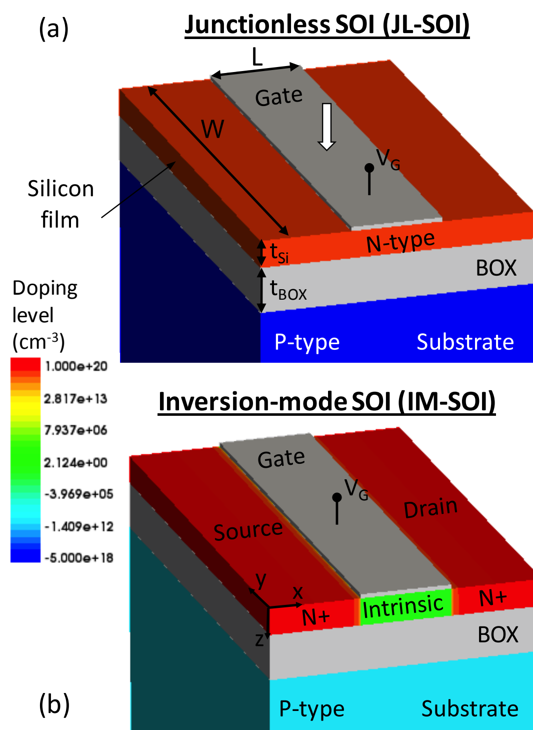
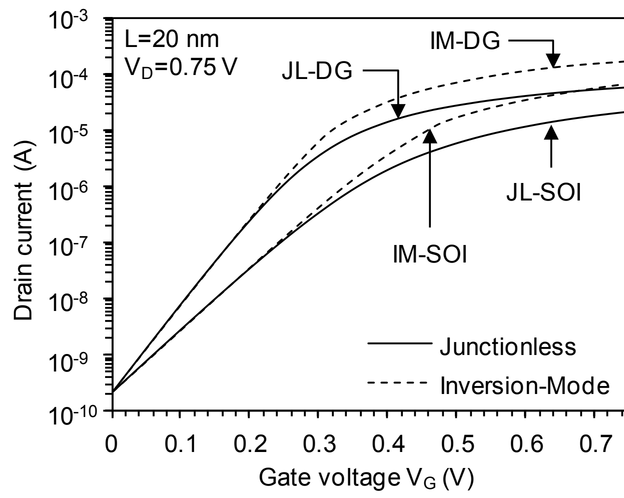


Figure 1. Munteanu and Autran.



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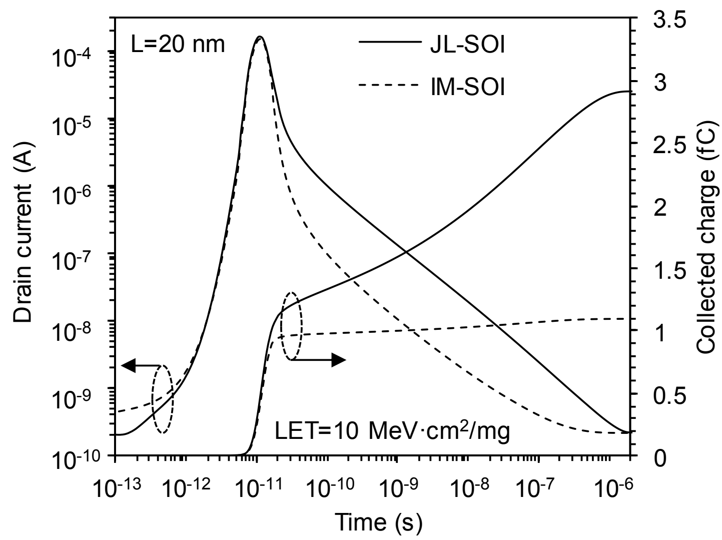

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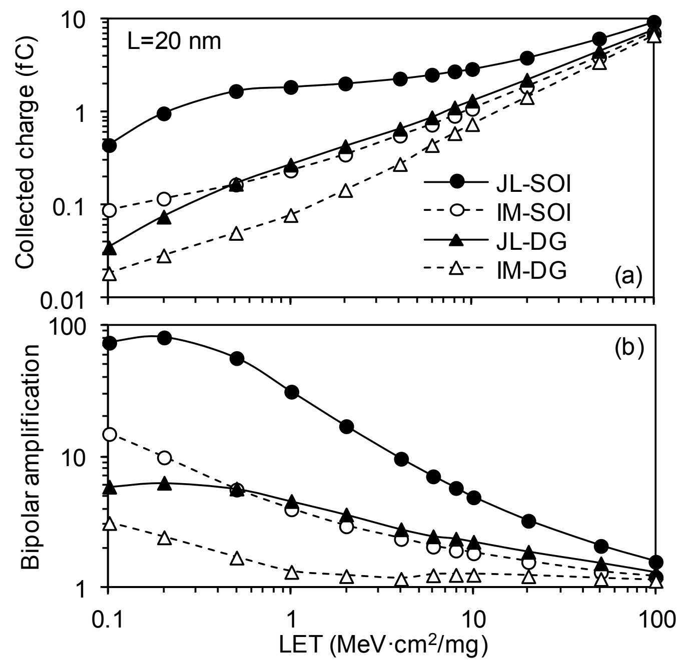

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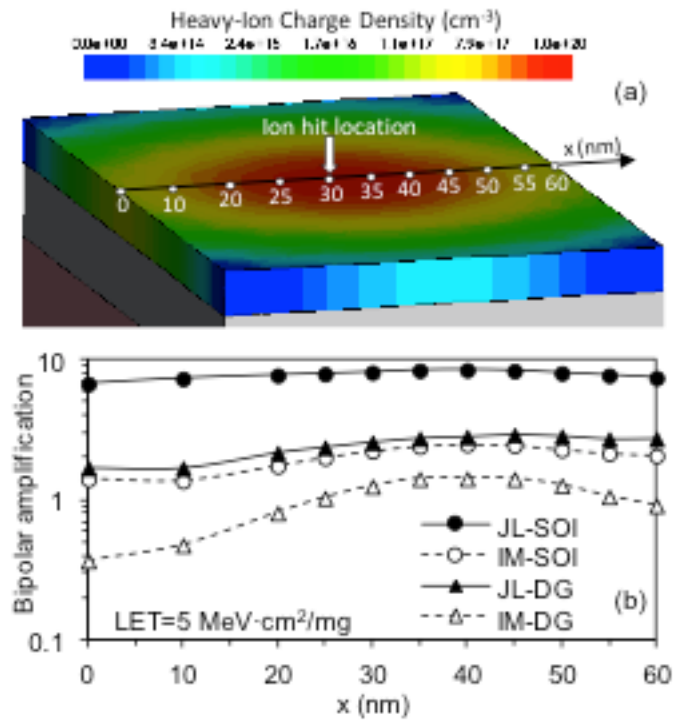

Figure 5. Munteanu and Autran.

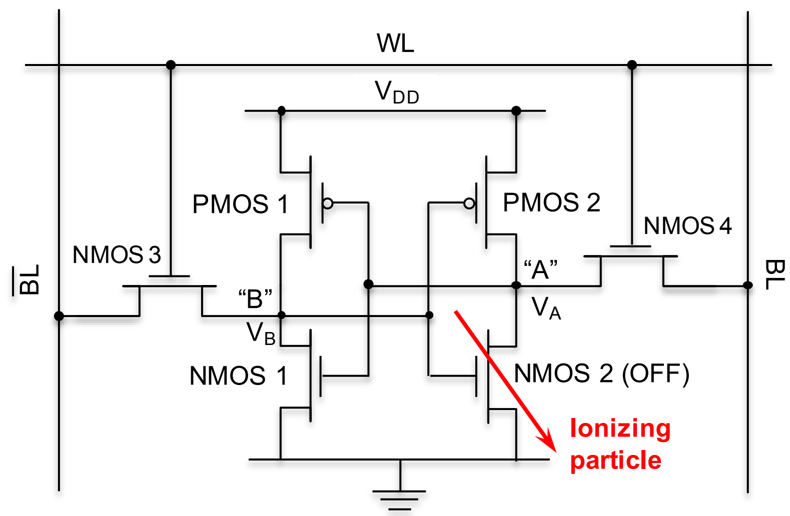

Figure 6. Munteanu and Autran.

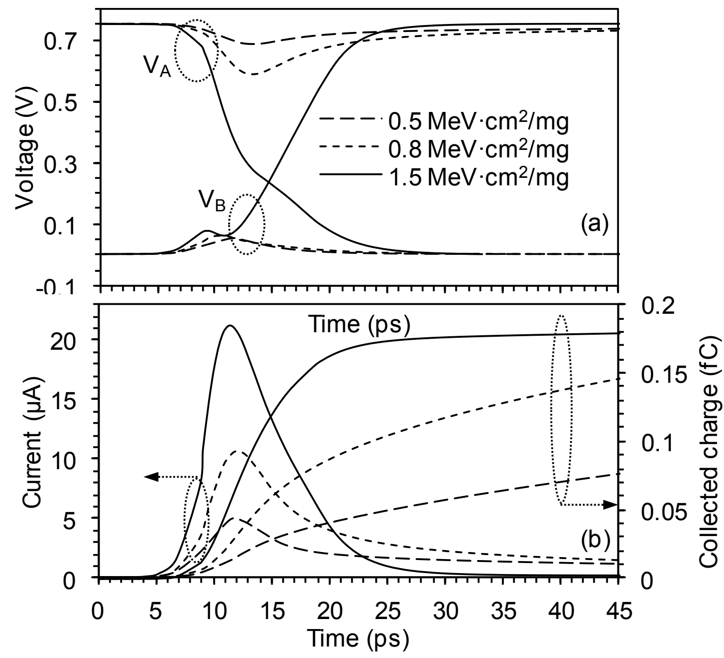

Figure 7. Munteanu and Autran.

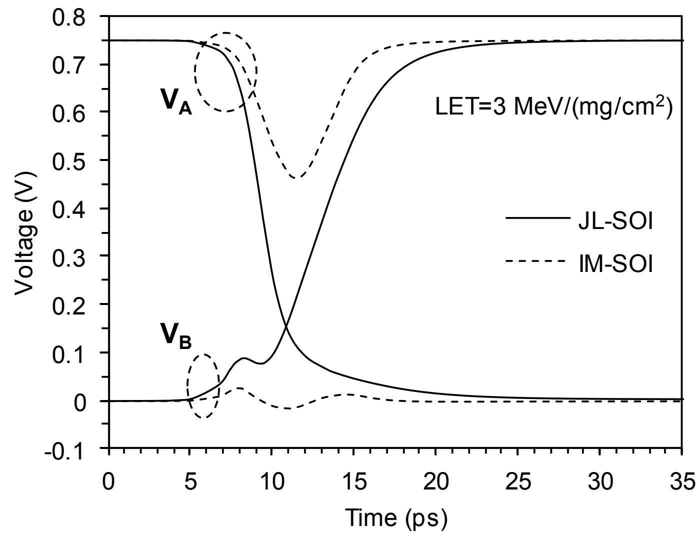

Figure 8. Munteanu and Autran.

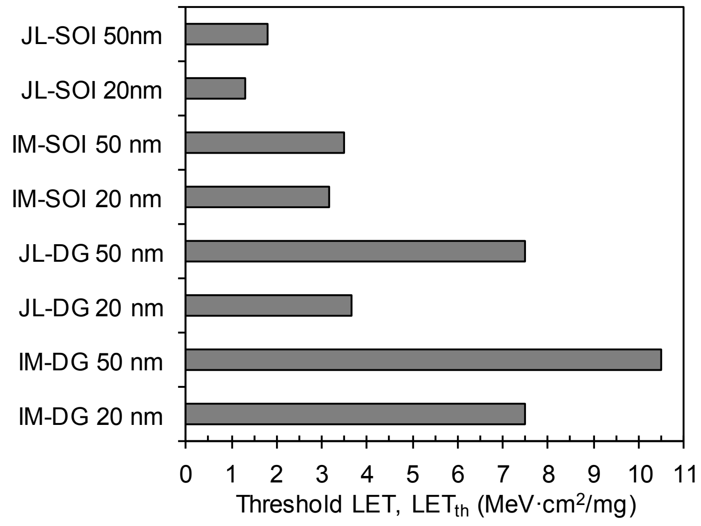

Figure 9. Munteanu and Autran.

Table I.

Film doping level (cm^{-3})	Critical charge (fC)	Threshold LET ($MeV \cdot cm^2/mg$)
5×10^{18}	0.158	1.95
1×10^{19}	0.126	1.32
1.5×10^{19}	0.110	0.86
2×10^{19}	0.104	0.75