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# Atmospheric radiation and COTS at ground level

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## Abstract

This tutorial will survey single event effects (SEE) induced by terrestrial cosmic rays on current commercial CMOS technologies. After describing the natural radiation environment at ground and atmospheric levels, the tutorial will describe the physics of SEEs, from the main mechanisms of interaction between atmospheric radiation (neutrons, protons, muons) and circuit materials to the electrical response of transistors, cells and complete circuits. SEE characterization using accelerated and real-time tests will be examined, as well as modeling and numerical simulation issues. Special emphasis will finally concern the radiation response of advanced technologies, including deca-nanometer bulk, FD-SOI and FinFET families.

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Microelectronics industry has experienced tremendous progress in the last forty years, especially with regard to the evolution of the products (i.e. integrated circuits) performances, and at the same time, concerning the drastic reduction of manufacturing costs per elementary integrated function. So far, this considerable growth of the semiconductor industry has been due to its technological capability to constantly miniaturize the elementary components of circuits, namely the MOSFET (metal-oxide-semiconductor field effect transistor), the basic building block of VLSI (very large scale integration) integrated circuits. However, the conventional bulk MOSFET scaling encountered this last decade serious physical and technological limitations, mainly related to the gate oxide ( $\text{SiO}_2$ ) leakage currents [1], the large increase of parasitic short channel effects and the dramatic mobility reduction [2] due to highly doped silicon substrates necessarily used to reduce these short channel effects. Technological solutions have been proposed in order to continue MOSFET miniaturization, such as: (i) the introduction of high-permittivity gate dielectric stacks [3], midgap metal gate and strained silicon channels [4]; (ii) the replacement of the conventional bulk MOSFET architecture by alternative solutions including the use of new materials (e.g. SOI materials) or new devices architectures (e.g. Multiple-Gate devices [5], silicon nanowire MOSFETs) allowing better electrostatic control, and, as a result, intrinsic channels with higher mobilities and currents.

As MOSFET scales have reduced, the sensitivity of the integrated circuits to radiation coming from the natural space or present in the terrestrial environment has been found to seriously evolve [6-8]. Nowadays, for ultra-scaled devices, natural radiation is inducing one of the highest failure rates of all reliability concerns for devices and circuits in the area of nanoelectronics [7]. In particular, ultra-scaled memory integrated circuits have been found to be more sensitive to single-event-upset (SEU) and digital devices more affected by digital single-event transient (DSETs). This sensitivity is a direct consequence of the reduction of device dimensions and spacing within memory cells combined with the reduction of supply voltage and node capacitance, resulting in a decrease of both the critical charge (i.e. the minimum amount of charge required to induce the flipping of the logic state) and the sensitive area (i.e. the minimum collection area inside which a given particle can deposit enough charge to induce a change in the cell) [7], [9].

This tutorial is structured in four main parts. In part 2, we will briefly describe the natural radiation environment at ground and atmospheric levels. The physics of SEEs will be summarized in part 3, from the main mechanisms of interaction between atmospheric radiation (neutrons, protons, muons) and circuit materials to the electrical response of transistors, cells and complete circuits. Part 4 will explain SEE characterization using accelerated and real-time tests, as well as modeling and numerical simulation issues. Finally, part 5 will present and discuss the radiation response of advanced commercial technologies, including deca-nanometer bulk, FD-SOI and FinFET families.

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